HITACHI

Displays, Hitachi, Ltd.

DATE : Oct. 10, 2001

COMPAL ELECTRONICS, Inc.

CUSTOMER'S ACCEPTANCE SPECIFICATIONS

TX46D15VC0CAA

CONTENTS

No.	ITEM	Sheet No.	Page
-	COVER	3284PS 2601-TX46D15VC0CAA-3	1-1/1
-	RECORD OF REVISION	3284PS 2602-TX46D15VC0CAA-3	2-1/1
-	DESCRIPTION	3284PS 2603-TX46D15VC0CAA-3	3-1/1
1	ABSOLUTE MAXMUM RATINGS	3284PS 2604-TX46D15VC0CAA-3	4-1/1
2	OPTICAL CHARACTERISTICS	3284PS 2605-TX46D15VC0CAA-3	5-1/2~2/2
3	ELECTRICAL CHARACTERISTICS	3284PS 2606-TX46D15VC0CAA-3	6-1/1
4	BLOCK DIAGRAM	3284PS 2607-TX46D15VC0CAA-3	7-1/1
5	INTERFACE PIN ASSIGNMENT	3284PS 2608-TX46D15VC0CAA-3	8-1/6~6/6
6	TIMING DUAGRAMS OF INTERFACE TIMING	3284PS 2609-TX46D15VC0CAA-3	9-1/3~3/3
7	DIMENSIONAL OUTLINE	3284PS 2610-TX46D15VC0CAA-3	10-1/2~2/2
8	DESIGNATION OF LOT MARK	3284PS 2611-TX46D15VC0CAA-3	11-1/1
9	COSMETIC SPECIFICATIONS	3284PS 2612-TX46D15VC0CAA-3	12-1/3~3/3
10	PRECAUTION	3284PS 2613-TX46D15VC0CAA-3	13-1/3~3/3

Accepted by _____

Proposed by K. Ogawa

RECORD OF REVISION

Date	The upper section : Before revision The lower section : After revision Sheet No.	Page	Summary
'01.09.20	3284PS 2605-TX46D15VC0CAA-1 3284PS 2605-TX46D15VC0CAA-2	5-1/2	Contrast Ratio Min.=150→180 Typ.=300→350
	3284PS 2605-TX46D15VC0CAA-1 3284PS 2605-TX46D15VC0CAA-2	5-1/2	Brightness of white Min.=160→180 Typ.=200→230
	3284PS 2605-TX46D15VC0CAA-1 3284PS 2605-TX46D15VC0CAA-2	8-4/6	Correction of errors in writing (pin.asign of TFT controlinput)
'01.10.10	3284PS 2605-TX46D15VC0CAA-2 3284PS 2605-TX46D15VC0CAA-3	5-1/2	Modititication of CR and Bwh C R:Min.=180→210 Typ.=230→235 Bwh:Min.=180→190 Typ.=230→235
	3284PS 2605-TX46D15VC0CAA-2 3284PS 2605-TX46D15VC0CAA-3	6-1/1	Moditication of VBL VBL:Min.=10.8→11.8 Typ.=12.0→12.5

DESCRIPTION

The following specifications are applied to the 18.1-inch Super-TFT module.

Note : Inverter for back light unit is built in a module.

Product Name : TX46D15VC0CAA

General Specifications

Effective Display Area	:(H)359.0×(V)287.2	(mm)
Number of Pixels	:(H)1280×(V)1024	(pixels)
Pixel Pitch	:(H)0.2805×(V)0.2805	(mm)
Color Pixel Arrangement	:R･G･B Vertical Stripe	
Display Mode	:Transmissive Mode Normally Black Mode	
Top Polarizer Type	:Anti-glare (Haze : 25%)	
Number of Colors	:16,777,216	(colors)
Viewing Angle Range	:Super Wide Version (Horizontal & Vertical : 170° , CR≧10)	
Input Signal	:2-channel LVDS (LVDS:Low Voltage Differential Signaling)	
Back Light	:8 pcs. of CCFL	
External Dimensions	:(H)389×(V)312×(t)33	(mm)
Weight	:max.2000 (typ. 1800)	(g)

1. ABSOLUTE MAXIMUM RATINGS

1.1 Environmental Absolute Maximum Ratings

ITEM	Operating		Storage		Unit	Note
	Min.	Max.	Min.	Max.		
Temperature	0	55	-20	60	℃	1)
Humidity	2)		2)		%RH	1)
Vibration	-	4.9(0.5G)	-	11.8 (1.2G)	m/s 2	3)
Shock	-	29.4(3G)	-	294 (30G)	m/s 2	4)
Corrosive Gas	Not Acceptable		Not Acceptable		-	
Illuminance of LCD Surface	-	50,000	-	50,000	lx	

Note 1) Temperature and Humidity should be applied to the glass surface of a Super-TFT module, not to the system installed with a module.
The temperature at the center of rear surface should be less than 60℃ on the condition of operating.
The brightness of a CCFL tends to drop at low temperature. Besides, the life-time becomes shorter at low temperature.

2)Ta≦ 40 ℃ · · · · · · Relative humidity should be less than 85%RH max. Dew is prohibited.
Ta＞ 40 ℃ · · · · · · Relative humidity should be lower than the moisture of the 85%RH at 40℃.

3)Frequency of the vibration is between 15Hz and 100Hz. (Remove the resonance point)

4)Pulse width of the shock is 10ms.

1.2 Electrical Absolute Maximum Ratings

(1)Super-TFT Module

Vss = 0 V

ITEM	SYMBOL	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	0	15.0	V	
Input Voltage for logic	V_I	-0.3	3.6	V	1)
Electrostatic Durability	V_{ESD0}	±100		V	2),3)
	V_{ESD1}	±8		kV	2),4)

Note 1)It is applied to pixel data signal and clock signal.
2)Discharge Coefficient : 200pF-250Ω, Environmental : 25℃-70%RH
3)It is applied to I/F connector pins.
4)It is applied to the surface of a metallic bezel and a LCD panel.

(2) Inverter

ITEM	SYMBOL	Maximum Rating	Unit	Note
Power Supply Voltage	VBL	14	V	
ON/OFF Signal L	VIL	-0.3	V	
ON/OFF Signal H	VIH	14	V	

2. OPTICAL CHARACTERISTICS

The following optical characteristics are measured under stable conditions. It takes about 30 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted. The optical characteristics should be measured in a dark room or equivalent state.

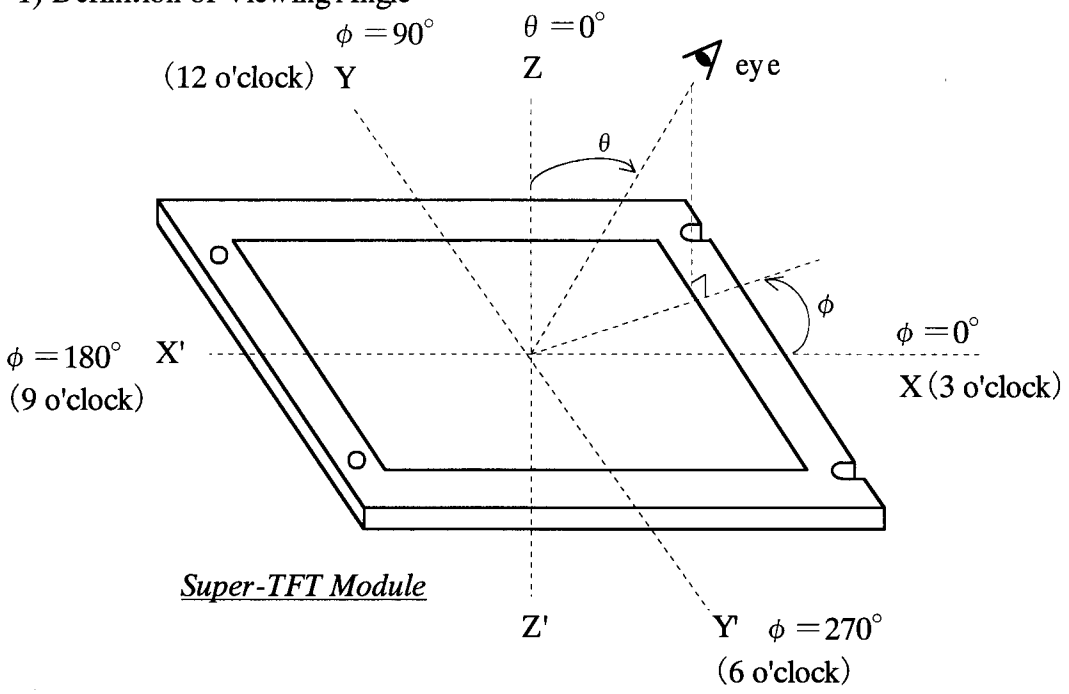
Measuring equipment : Prichard 1980A, or equivalent

Temperature of LCD surface = 25℃,、VDD = 12.0V、f V = 60Hz、

VBL=12V, BC=GND

ITEM		SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT	NOTE
Contrast Ratio		CR	θ =0° 1)	210	350	—	—	2)
Response Time	Rise	ton		—	15	30	ms	3)
	Fall	toff		—	15	30	ms	3)
Brightness of white		Bwh		190	235	—	cd/m²	
Brightness uniformity		Buni		—	—	20	%	4)
Color Chromaticity (CIE)	Red	χ		0.58	0.63	0.68	—	[Gray scale =255]
		y		0.29	0.34	0.39		
	Green	χ		0.23	0.28	0.33		
		y		0.56	0.61	0.66		
	Blue	χ		0.09	0.14	0.19		
		y		0.04	0.09	0.14		
	White	χ		0.25	0.30	0.35		
		y		0.27	0.32	0.37		
Variation of Color Position (CIE)	Red	Δχ	θ =+50° φ =0° 、90° 180° 、270° 1)	—	—	0.04	—	5) [Gray scale =255]
		Δy		—	—	0.04		
	Green	Δχ		—	—	0.04		
		Δy		—	—	0.04		
	Blue	Δχ		—	—	0.04		
		Δy		—	—	0.04		
	White	Δχ		—	—	0.04		
		Δy		—	—	0.04		
Contrast Ratio at 85°		CR85°	θ =85°	10	—	—	—	

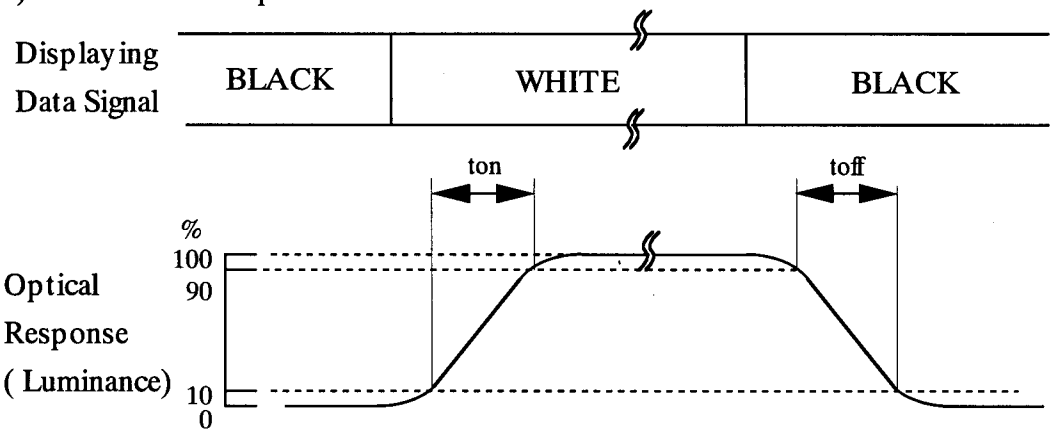
Note 1) Definition of Viewing Angle



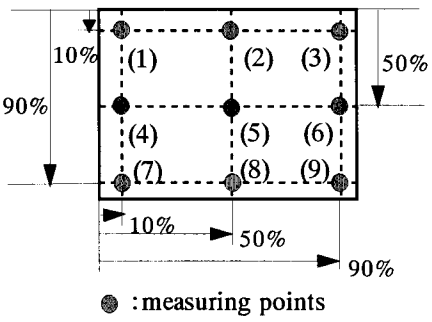
2) Definition of Contrast Ratio (CR)

$$CR = \frac{\text{(Luminance at displaying WHITE)}}{\text{(Luminance at displaying BLACK)}}$$

3) Definition of Response Time



4) Definition of Brightness Uniformity



Display pattern is white (255 level) and gray scale. The brightness uniformity is defined as the following equation. Brightness at each point is measured, and average, maximum and minimum brightness is calculated.

$$Buni = \frac{|Bmax \text{ or } Bmin - Bave|}{Bave} \times 100$$

where, Bmax = Maximum brightness

Bmin = Minimum brightness

$$Bave = \text{Average brightness} = \frac{\sum_{k=1}^{9} (B(k))}{9}$$

5) Variation of color position on CIE is defined as difference between colors at $\theta = 0°$ and at $\theta = 50°$ & $\phi = 0°$,90° ,180° ,270° .

3. ELECTRICAL CHARACTERISTICS

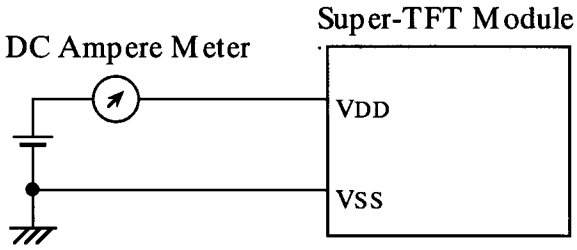
3.1 TFT-LCD Module

Ta=25℃, Vss=0V

ITEM	SYMBOL	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	VDD	10.8	12	13.2	V	
Power Supply Current	IDD	—	—	700	mA	1),2)
Vsync Frequency	fv	—	60	—	Hz	
Hsync Frequency	fH	—	—	—	kHz	
DCLK Frequency	fCLK	50	54	60	MHz	
Input Signals	VI	—	—	—	V	3)

Dimensions in parentheses are reference value.

Note 1) DC current at fv=60Hz, fCLK=54MHz and VDD=12.0V



2) Current fuse(1.6A,24V:Product Name ;JAA2402162NA, Matsuo Corp.) is built in a module. Current capacity of power supply for VDD should be larger than 4A, so that the fuse can be opened at the trouble of power supply.
3) The picture on maximum current is white picture.
4) Characteristics of input signals are shown in LVDS data sheets. (Receiver:THC63LVDF84A or DS90cf386)

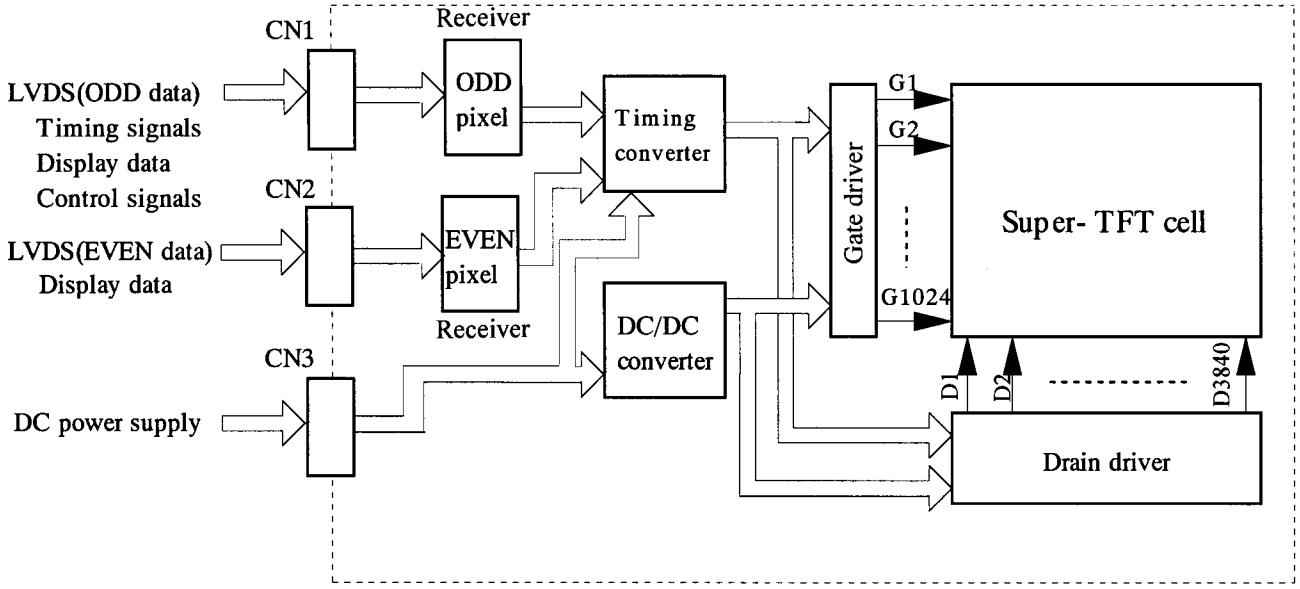
3.2 Inverter (Back Light)

ITEM	SYMBOL	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	VBL	11.8	12.5	13.2	V	
Power Supply Current	IBL	—	(2.8)	(3.3)	A	VBL=12V
Kick-Off Current	—	—	(2.8)	(3.3)	A	
Dimming voltage	VBCH	3.3	—	—	V	Min. dimming
	VBCL	—	—	0	V	Max. dimming
ON/OFF Signal L	VIL	0	—	0.8	V	OFF state
ON/OFF Signal H	VIH	2	—	5	V	ON state
Frequency	f0	49	54	59	kHz	
Dimming Frequency	fB	234	260	286	Hz	
Dimming Range	—	20	—	100	%	1)

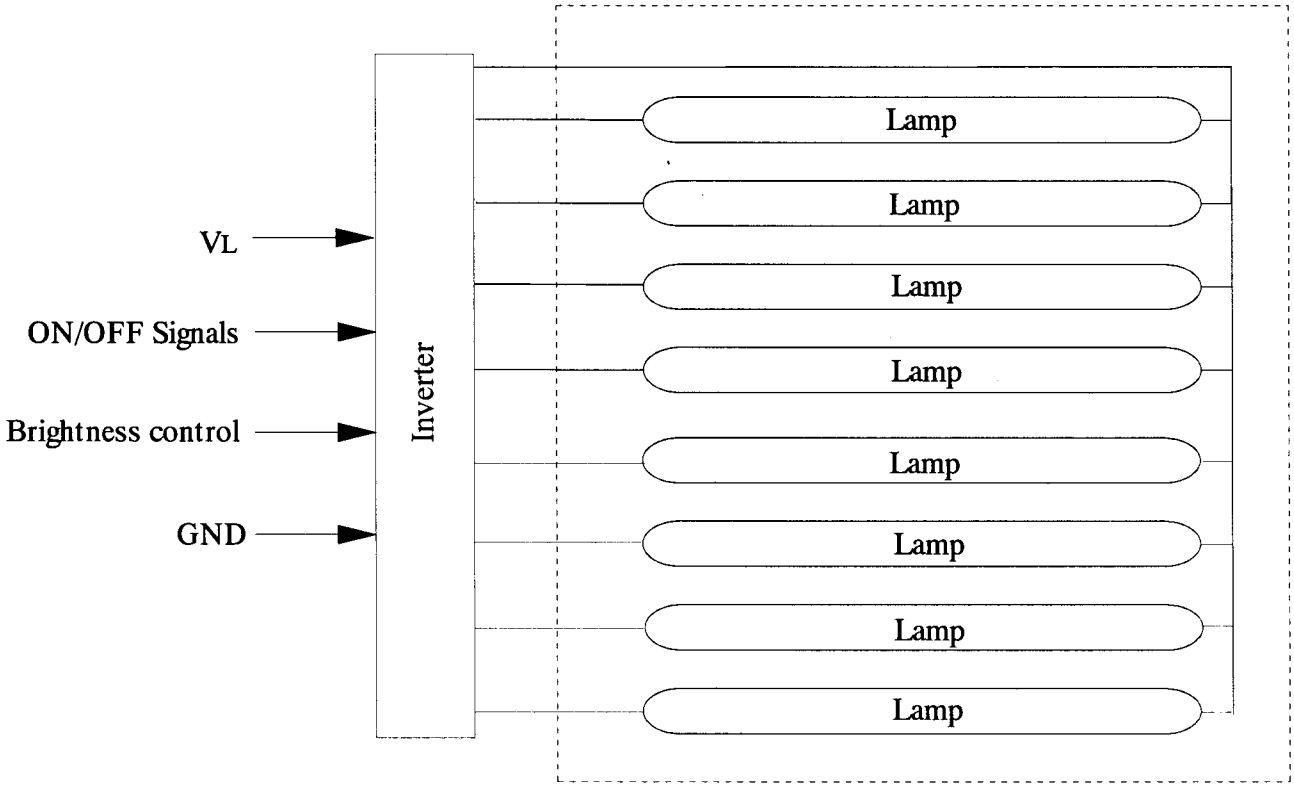
Notes 1) 100 % mean the maximum brightness.

4. BLOCK DIAGRAM

(1) Super-TFT Module



(2) Back light unit



Note) The inverter for driving CFLs is not built in a module.

5. INTERFACE PIN ASSIGNMENT

CN1 : JAE FI-SE20P-HF
(Matching connector: JAE FI-SE20M)

Pin No.	SYMBOL	Function	
1	(NC)		
2	(NC)		
3	Vss	GND(0V)	1)
4	Vss		
5	RAIN0-	Odd pixel data	2)
6	RAIN0+		
7	Vss	GND(0V)	1)
8	RAIN1-	Odd pixel data	2)
9	RAIN1+		
10	Vss	GND(0V)	1)
11	RAIN2-	Odd pixel data	2)
12	RAIN2+		
13	Vss	GND(0V)	1)
14	RACLKIN-	Odd pixel data	2)
15	RACLKIN+		
16	Vss	GND(0V)	1)
17	RAIN3-	Odd pixel data	2)
18	RAIN3+		
19	Vss	GND(0V)	1)
20	RSVD		

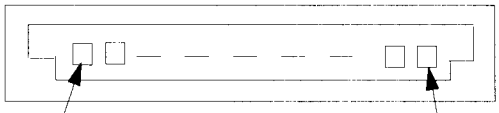
CN2 : JAE FI-SE20P-HF
(Matching connector: JAE FI-SE20M)

ﾋﾟﾝ No.	SYMBOL	Function	
1	(NC)		
2	(NC)		
3	Vss	GND(0V)	1)
4	Vss		
5	RBIN0-	Even pixel data	2)
6	RBIN0+		
7	Vss	GND(0V)	1)
8	RBIN1-	Even pixel data	2)
9	RBIN1+		
10	Vss	GND(0V)	1)
11	RBIN2-	Even pixel data	2)
12	RBIN2+		
13	Vss	GND(0V)	1)
14	RBCLKIN-	Even pixel data	2)
15	RBCLKIN+		
16	Vss	GND(0V)	1)
17	RBIN3-	Even pixel data	2)
18	RBIN3+		
19	Vss	GND(0V)	1)
20	RSVD		

Notes 1) All Vss pins should be grounded.

2) RnINm+ and RnINm- (n=A、B m=0、1、2、3) should be wired by twist-pairs or side-by-side FPC patterns, respectively.

3) Pin assignment of CN1 and CN2 is as follows.



(Figure from top-view)

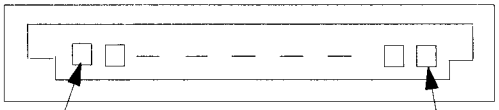
CN3:JAE LZ-10P-SL-SMT (Matching connector:JAE LZ-10S-SC3)

Pin No.	SYMBOL	Function
1	VDD	Power supply (typ.12V) 1)
2	VDD	
3	VDD	
4	(NC)	
5	(NC)	
6	VSS	GND(0V) 2)
7	VSS	
8	VSS	
9	(NC)	
10	(NC)	

Notes 1) All VDD pins should be connected to +12.0 V(typ.).

2) All Vss pins should be grounded.

3) Pin assignment of CN3 is as follows.



10pin (Figure from top-view) 1pin

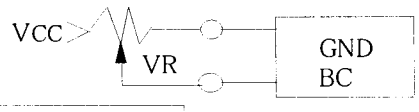
CN4:S12B-PH-SM3-TB(JST) (Matching connector:JST PHR-12)

Pin No.	SYMBOL	Function
1	V_{BL}	Power supply (typ.12V) 1)
2	V_{BL}	
3	V_{BL}	
4	V_{BL}	
5	ON/OFF	Remote ON/OFF Switch ON:VIH、OFF:VIL
6	GND	GND(0V) 2)
7	GND	
8	BC	Brightness Control BC=GND:max brightness、BC=VCC:min brightness 3)
9	GND	GND(0V) 2)
10	GND	
11	GND	
12	GND	

Notes 1) All VBL pins should be connected to +12.0 V(typ.).

2) All GND pins should be grounded (0V).

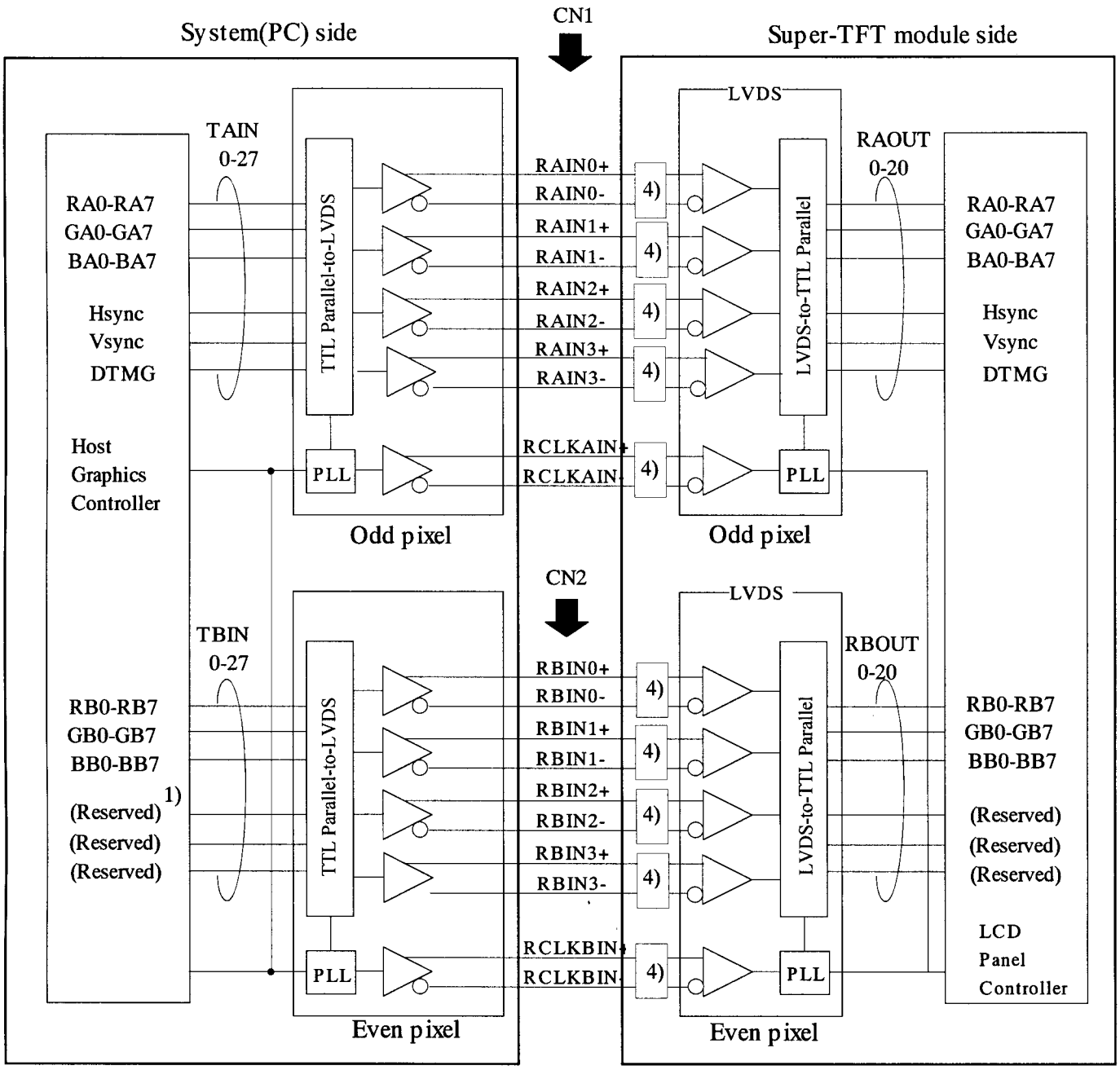
3) VR should be setted 5 to 20 kΩ. VCC=3.3V



4) Pin assignment is as follows.

1pin (Figure from top-view) 12pin

BLOCK DIAGRAM OF INTERFACE



Receiver : THC63LVDF84A by Thine,
DS90CF386 by NS

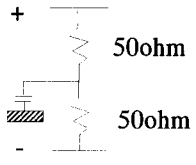
RA0-7, RB0-7 : R data
GA0-7, GB0-7 : G data
BA0-7, BB0-7 : B data
Hsync :Horizontal synchronization
Vsync:Vertical synchronization
DTMG : Display timing data

Notes 1) RSVD(reserved) pins on a transmitter should be connected with Vss.

2) The system must have a LVDS transmitter(THC63LVDM83A, DS90C385) to drive a module.

3) The impedance of LVDS cable should be 50 ohms per a signal line or about 100 ohms per a twist-pair line when it is used differentially.

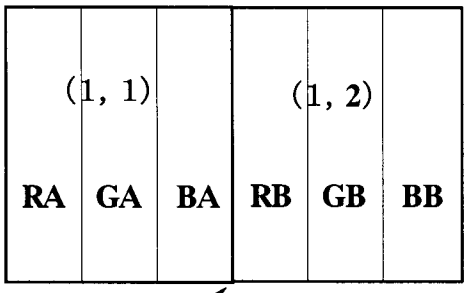
4) LVDS terminal circuit of a module is as follows.



LVDS INTERFACE

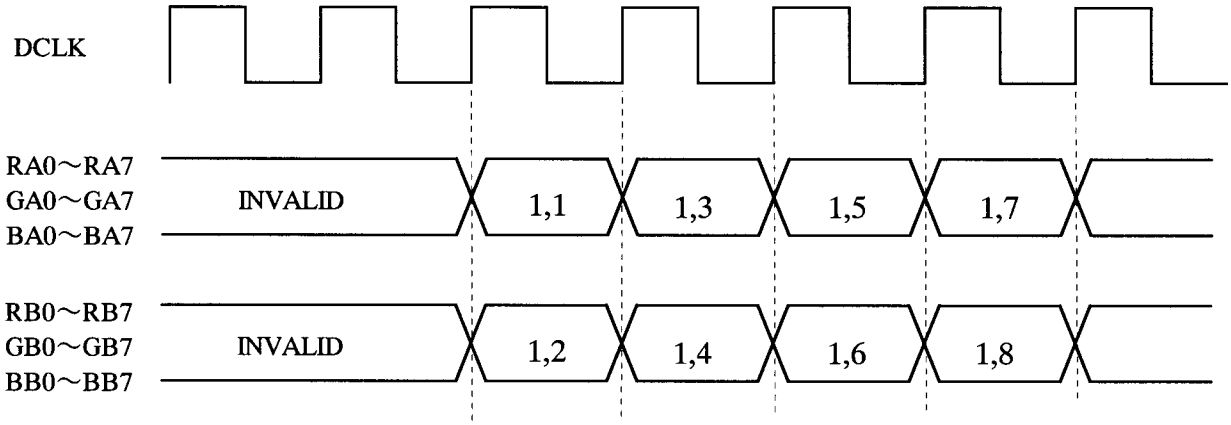
	INPUT SIGNAL	Transmitter		Interface connector		Receiver THC63LVDF84A		TFT control input
		pin	INPUT	System side	Super-TFT modu	pin	OUTPUT	
LVDS Odd	RA0	51	TAIN0	TA OUT0+	RA IN0+	27	RAOUT0	RA0
	RA1	52	TAIN1			29	RAOUT1	RA1
	RA2	54	TAIN2			30	RAOUT2	RA2
	RA3	55	TAIN3			32	RAOUT3	RA3
	RA4	56	TAIN4			33	RAOUT4	RA4
	RA5	3	TAIN6	TA OUT0-	RA IN0-	35	RAOUT6	RA5
	GA0	4	TAIN7			37	RAOUT7	GA0
	GA1	6	TAIN8	TA OUT1+	RA IN1+	38	RAOUT8	GA1
	GA2	7	TAIN9			39	RAOUT9	GA2
	GA3	11	TAIN12			43	RAOUT12	GA3
	GA4	12	TAIN13			45	RAOUT13	GA4
	GA5	14	TAIN14	TA OUT1-	RA IN1-	46	RAOUT14	GA5
	BA0	15	TAIN15			47	RAOUT15	BA0
	BA1	19	TAIN18			51	RAOUT18	BA1
	BA2	20	TAIN19	TA OUT2+	RA IN2+	53	RAOUT19	BA2
	BA3	22	TAIN20			54	RAOUT20	BA3
	BA4	23	TAIN21			55	RAOUT21	BA4
	BA5	24	TAIN22			1	RAOUT22	BA5
	HSYNC	27	TAIN24			3	RAOUT24	HSYNC
	VSYNC	28	TAIN25	TA OUT2-	RA IN2-	5	RAOUT25	VSYNC
	DTMG	30	TAIN26			6	RAOUT26	DTMG
	RA6	50	TAIN27	TA OUT3+	RA IN3+	7	RAOUT27	RA6
	RA7	2	TAIN5			34	RAOUT5	RA7
	GA6	8	TAIN10			41	RAOUT10	GA6
	GA7	10	TAIN11			42	RAOUT11	GA7
	BA6	16	TAIN16			49	RAOUT16	BA6
	BA7	18	TAIN17	TA OUT3-	RA IN3-	50	RAOUT17	BA7
	RSVD 1)		TAIN23			2	RAOUT23	RSVD
	DCLK	25	TCLKA IN	TCLKA OUT+	RCLKA IN+	26	RCLKA OUT	DCLK
		31		TCLKA OUT-	RCLKA IN-			
LVDS Even	RB0	51	TBIN0	TB OUT0+	RB IN0+	27	RBOUT0	RB0
	RB1	52	TBIN1			29	RBOUT1	RB1
	RB2	54	TBIN2			30	RBOUT2	RB2
	RB3	55	TBIN3			32	RBOUT3	RB3
	RB4	56	TBIN4			33	RBOUT4	RB4
	RB5	3	TBIN6	TB OUT0-	RB IN0-	35	RBOUT6	RB5
	GB0	4	TBIN7			37	RBOUT7	GB0
	GB1	6	TBIN8	TB OUT1+	RB IN1+	38	RBOUT8	GB1
	GB2	7	TBIN9			39	RBOUT9	GB2
	GB3	11	TBIN12			43	RBOUT12	GB3
	GB4	12	TBIN13			45	RBOUT13	GB4
	GB5	14	TBIN14	TB OUT1-	RB IN1-	46	RBOUT14	GB5
	BB0	15	TBIN15			47	RBOUT15	BB0
	BB1	19	TBIN18			51	RBOUT18	BB1
	BB2	20	TBIN19	TB OUT2+	RB IN2+	53	RBOUT19	BB2
	BB3	22	TBIN20			54	RBOUT20	BB3
	BB4	23	TBIN21			55	RBOUT21	BB4
	BB5	24	TBIN22			1	RBOUT22	BB5
	RSVD 1)	27	TBIN24			3	RBOUT24	RSVD
	RSVD 1)	28	TBIN25	TB OUT2-	RB IN2-	5	RBOUT25	RSVD
	RSVD 1)	30	TBIN26			6	RBOUT26	RSVD
	RB6	50	TBIN27	TB OUT3+	RB IN3+	7	RBOUT27	RB6
	RB7	2	TBIN5			34	RBOUT5	RB7
	GB6	8	TBIN10			41	RBOUT10	GB6
	GB7	10	TBIN11			42	RBOUT11	GB7
	BB6	16	TBIN16			49	RBOUT16	BB6
	BB7	18	TBIN17	TB OUT3-	RB IN3-	50	RBOUT17	BB7
	RSVD 1)		TBIN23			2	RBOUT23	RSVD
	DCLK	25	TCLKB IN	TCLKB OUT+	RCLKB IN+	26	RCLKB OUT	DCLK
		31		TCLKB OUT-	RCLKB IN-			

CORRESPONDENCE BETWEEN INPUT DATA AND DISPLAY IMAGE



Odd pixel : RA0～RA7 : R data
GA0～GA7 : G data
BA0～BA7 : B data
Even pixel : RB0～RB7 : R data
GA0～GA7 : G data
BB0～BB7 : B data

1,1	1,2	1,3	----------	1,1280
2,1	2,2	2,3	----------	2,1280
3,1	3,2	3,3	----------	3,1280
⋮	⋮	⋮		⋮
1024,1	1024,2	1024,3	----------	1024,1280



RELATIONSHIP BETWEEN DISPLAY COLORS AND INPUT SIGNALS

Color \ Input data		R data								G data								B data							
		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
		MSB							LSB	MSB							LSB	MSB							LSB
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	CYAN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	MAGENDA	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	RED(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	GREEN(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:		:	:	0	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:		:	:	0	:	:	:	:	:	:	:	:
	GREEN(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
BLUE	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	BLUE(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	BLUE(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Notes 1) Definition of gray scale : Color (n)

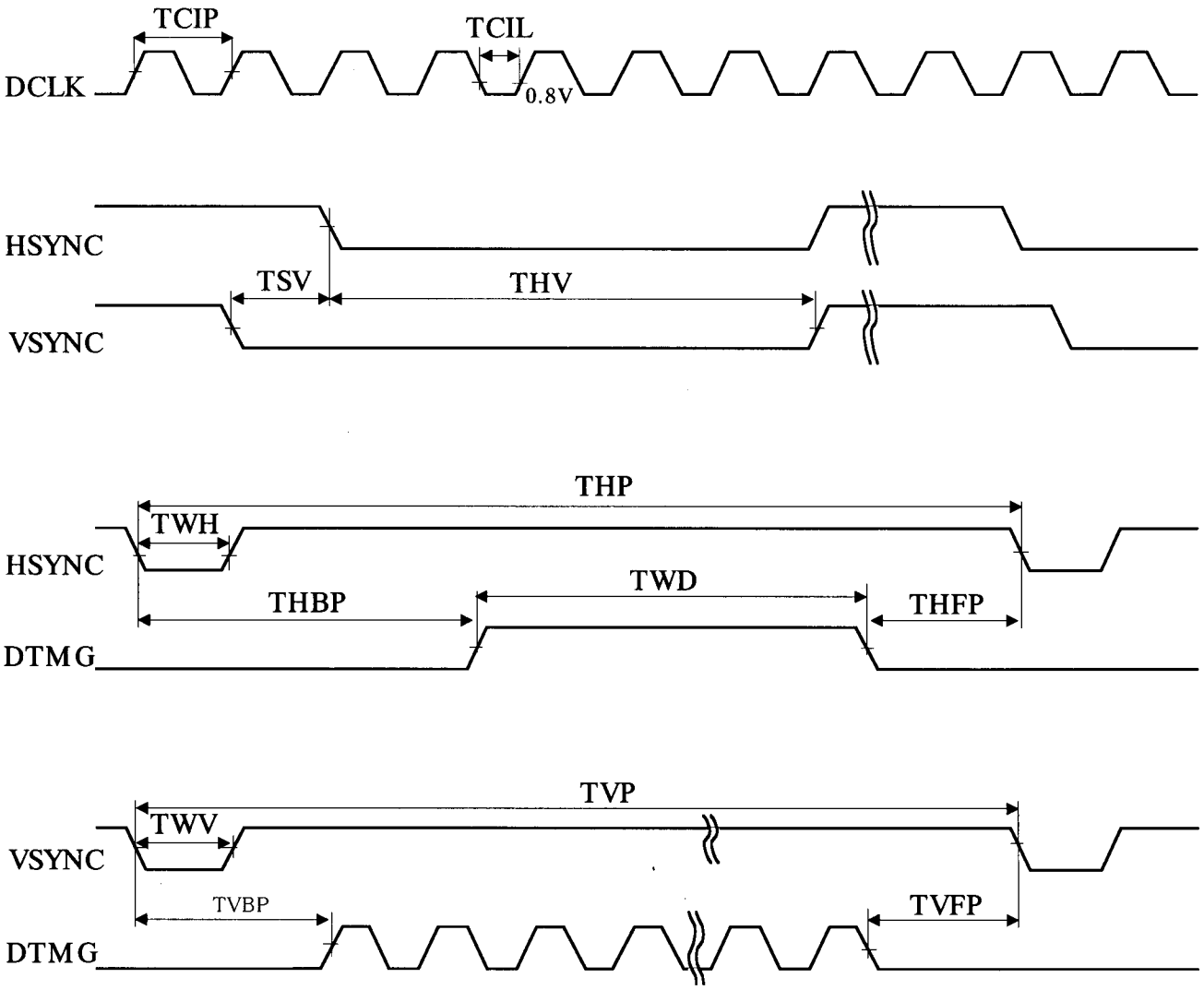
n indicates gray scale level. Higher n means brighter level.

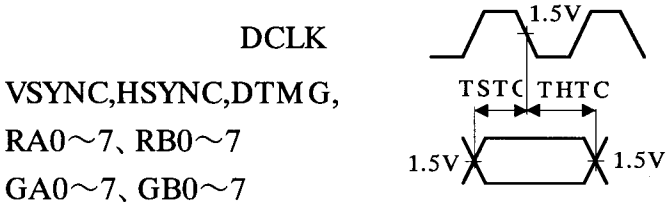
2) Data signals : 1:High, 0:Low

6. TIMING DIAGRAMS OF INTERFACE TIMING

6.1 Timing chart

The following timing chart is defined at input of a LVDS transmitter.





Notes 1) Reference level of timing signals is 1.5 V unless it is stated on the chart. However, high level voltage (V_{IH}) and low level voltage (V_{IL}) are defined as follows:

$V_{IH} \geqq 2.0V$ $V_{IL} \leqq 0.8V$

The above definitions come from specifications of THC63LVDM83A(Thine) or DS90C385(Ns).

2) The timing of DCLK to other signals comes from specifications of THC63LVDM83A or DS90C385. It is recommended to check specifications of the LVDS.

3) HSYNC and VSYNC is a timing in negative polarity.

6.2 INTERFACE TIMING SPECIFICATIONS

ITEM		SYMBOL	Min.	Typ.	Max.	Unit	Notes
DCLK	Period	TCIP	17.6	18.5	19.4	ns	
	Duty	D	0.4	0.5	0.6	-	D=TCIL/TCIP
HSYNC	Period	THP	728	832	1200	TCIP	
	Width-active	TWH	8	-	120	TCIP	
VSYNC	Set up time	TSV	0	-	-	TCIP	to HSYNC
	Hold time	THV	2	-	-	TCIP	to HSYNC
	Period	TVP	1027	1078	2000	THP	
	Width-active	TWV	1	-	120	THP	
DTMG	Horizontal back porch	THBP	110	176	1)	TCIP	
	Horizontal front porch	THFP	0	16	1)	TCIP	
	Vertical back porch	TVBP	0	-	2)	THP	
	Vertical front porch	TVFP	3	-	2)	THP	
	Width-active	TWD	640	-	-	TCIP	
COMMON	Set up time	TSTC	6	-	3)	ns	
	Hold time	THTC	2	-	3)	ns	

Notes 1) THBP+THFP≦560 TCIP

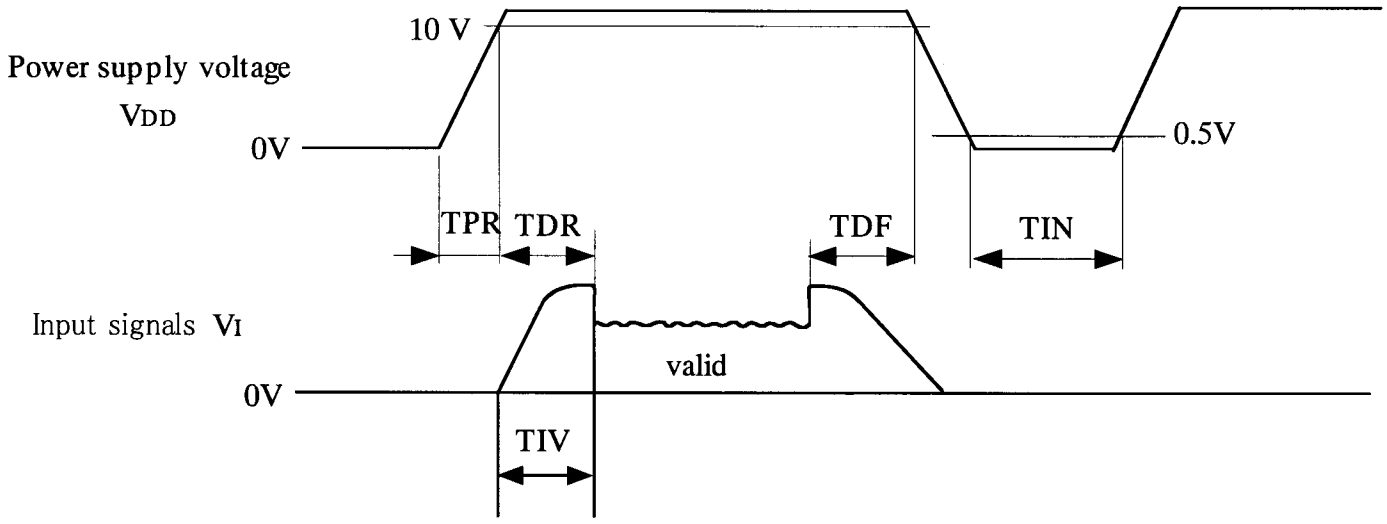
2) TVBP+TVFP≦253 THP

3) TSTC and THTC come from a specifications of a LVDS transmitter. It is recommended to specifications of a LVDS transmitter.

4) fV=1/TVP≦60Hz (see 3. Description).

5) fH=1/THP≦64.9kHz (see 3. Description).

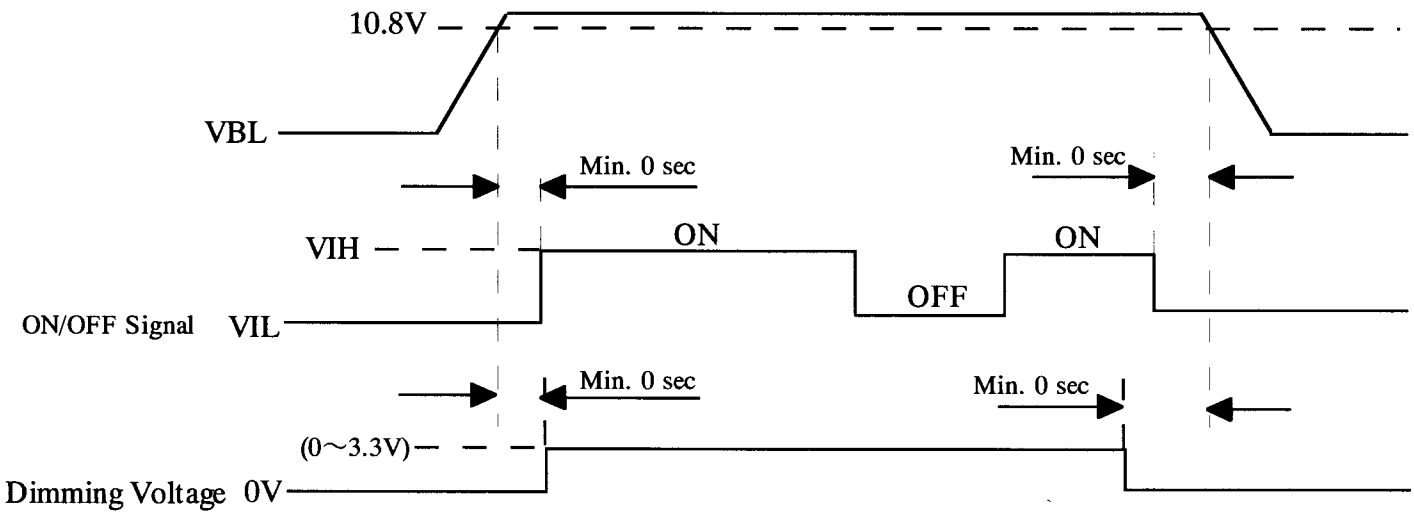
6.3 TIMING BETWEEN INTERFACE SIGNALS AND POWER SUPPLY



Timing of power supply voltage and input signals should be used under the following specifications.

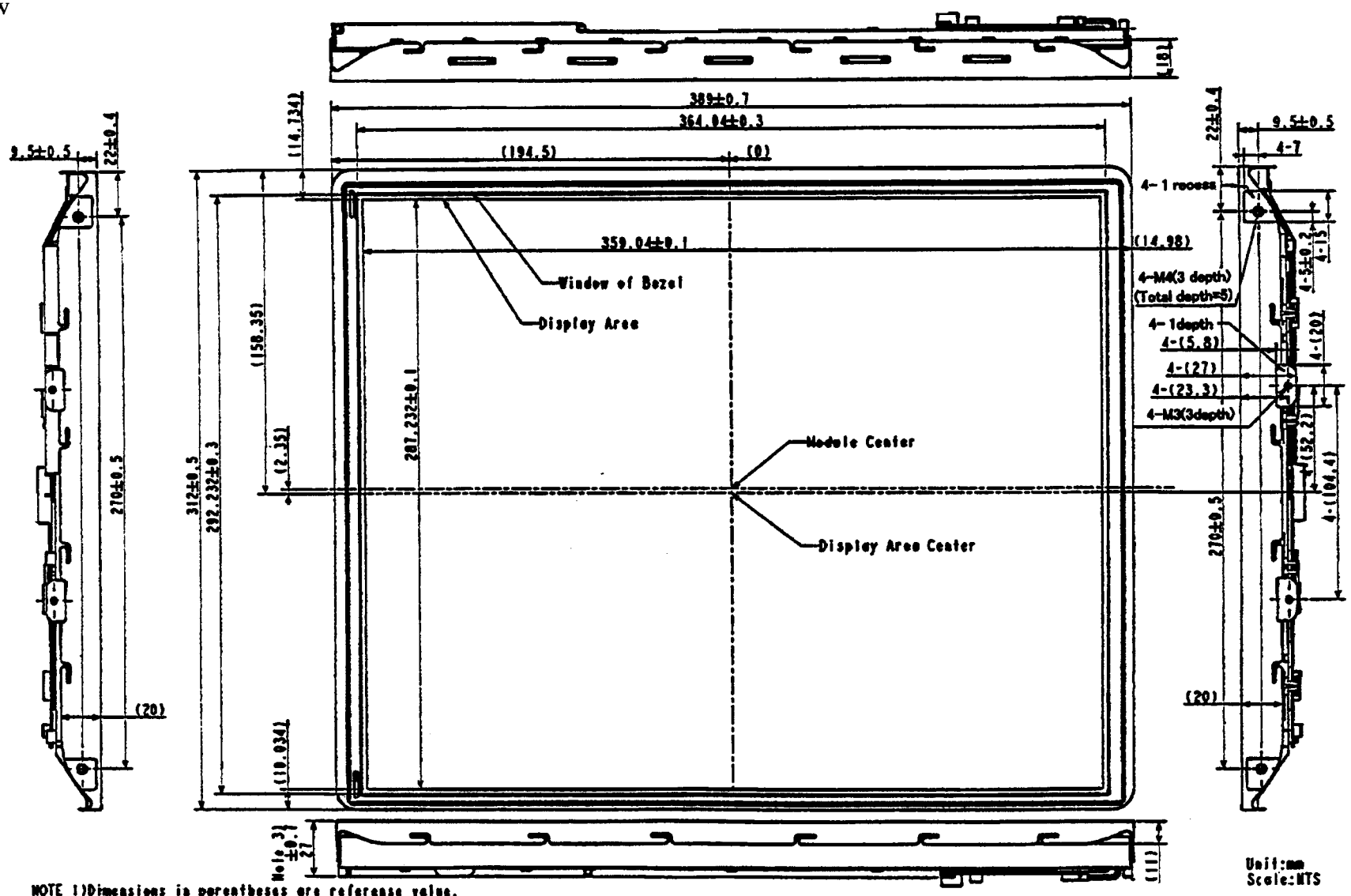
0ms ≦ TPR ≦ 30ms
0ms ≦ TDR ≦ 500ms
0ms ≦ TDF ≦ 500ms
TIN ≧ 500ms
TIV ≦ 3ms

(2) Inverter



Note 1) ON/OFF signal and dimming voltage is not specified during VBL=high (≧10.8V).
However, specifications referred to Sec.3 must be satisfied.
2) Dimming voltage should be 0V during VBL=low (<10.8V).

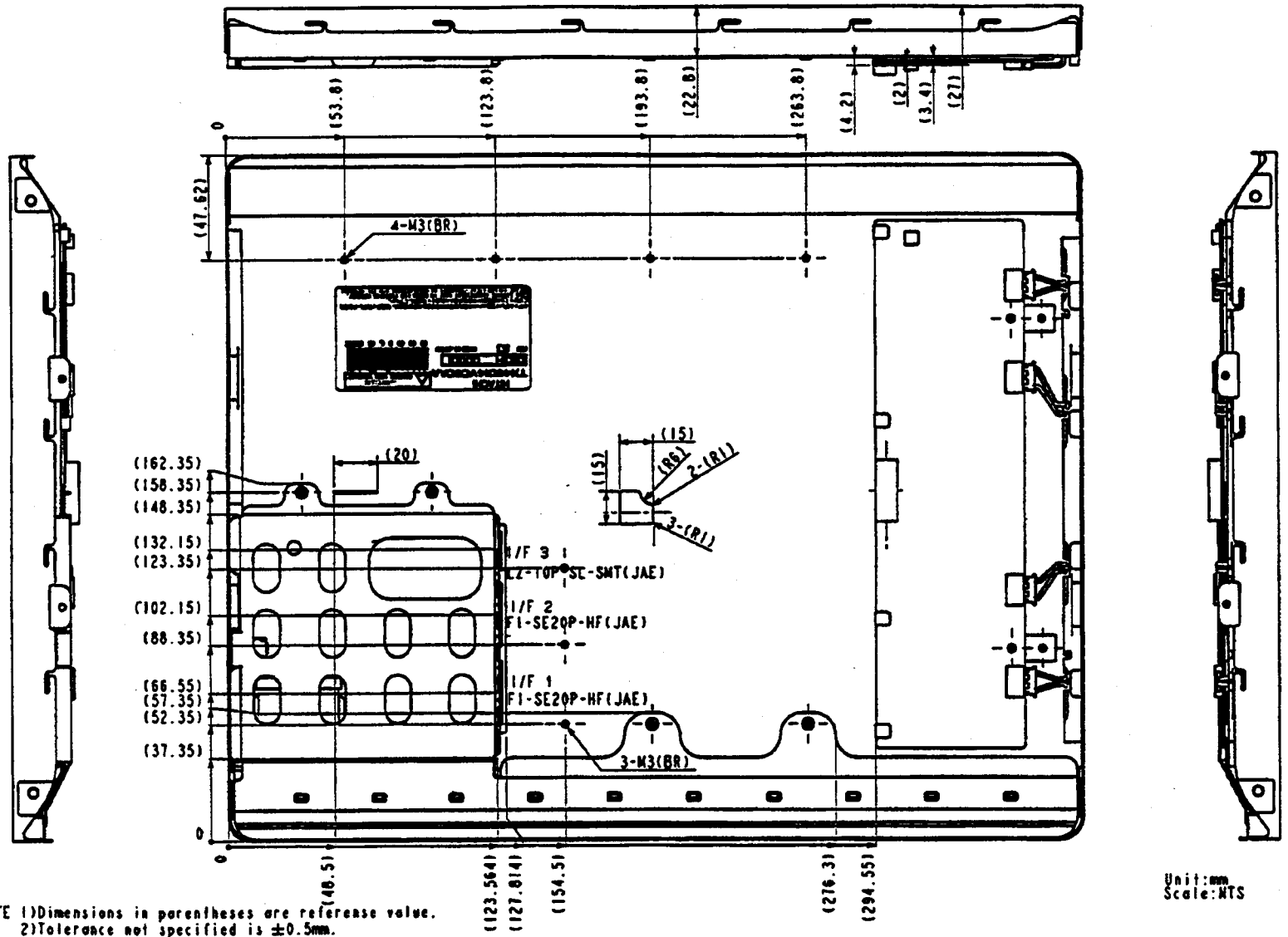
TX46D15VC0CAA
EXTERNAL DIMENSIONAL
Front View



NOTE 1)Dimensions in parentheses are reference value.
2)Tolerance not specified is ±0.5mm.
3)Measure the values 9.8x10^4Pa(1.0kgf/cm^2).

Displays,Hitachi,Ltd.	Date	Oct. 10, 2001	Sheet No.	3284PS 2610-TX46D15VC0CAA-3	10-1/2

TX46D15VC0CAA
EXTERNAL DIMENSIONAL
Rear View



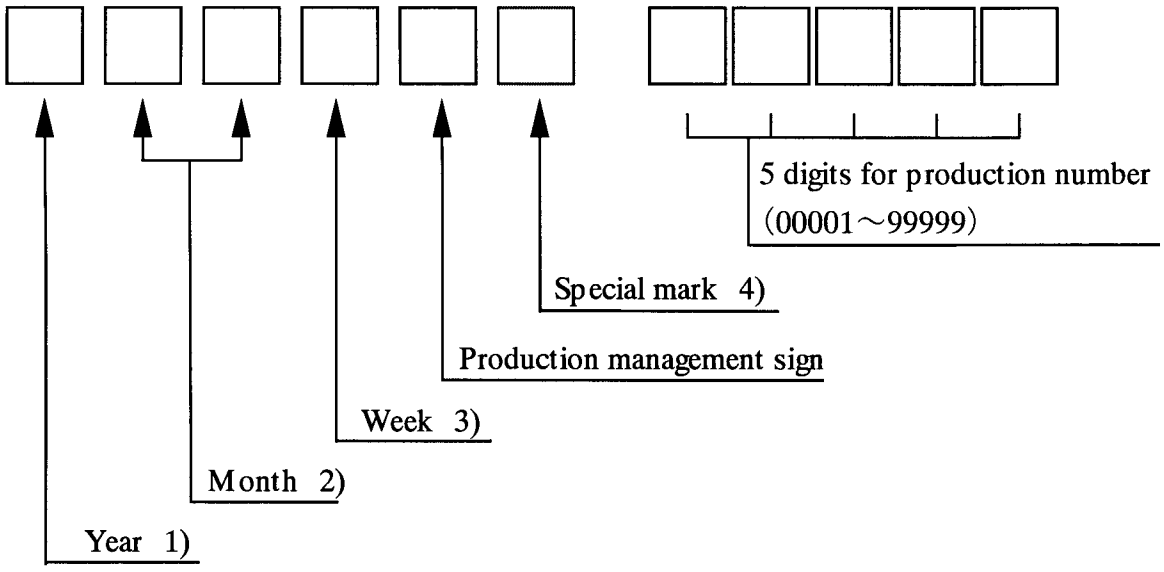
NOTE 1)Dimensions in parentheses are reference value.
2)Tolerance not specified is ±0.5mm.
3)Measure the values 9.8×10^4Pa(1.0kgf/cm^2).

Unit:mm
Scale:NTS

Displays,Hitachi,Ltd.	Date	Oct. 10, 2001	Sheet No.	3284PS 2610-TX46D15VC0CAA-3	10-2/2

8. DESIGNATION OF LOT MARK

8.1 LOT MARK



Notes

1)

Year	Mark
1999	9
2000	0
2001	1
2002	2

2)

Month	Mark	Month	Mark
1	01	7	07
2	02	8	08
3	03	9	09
4	04	10	10
5	05	11	11
6	06	12	12

3)

Week (Day)	Mark
1～7	1
8～14	2
15～21	3
22～28	4
29～31	5

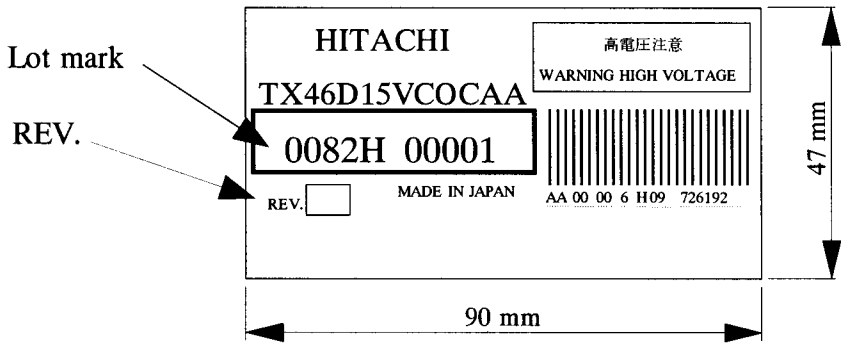
4) It is the mark that was opened up by production person to take correspondence with production number.

8.2 Revision (REV.) control

REV. is the column for manufacturing convenience. A-Z except I and O may be written on this column.

8.3 Location of lot mark

Lot mark is printed on a label. The label is on the metallic bezel as shown in 7. External Dimensional. The style of character will be changed without notice.



9. COSMETIC SPECIFICATIONS

9.1 Condition for cosmetic inspection

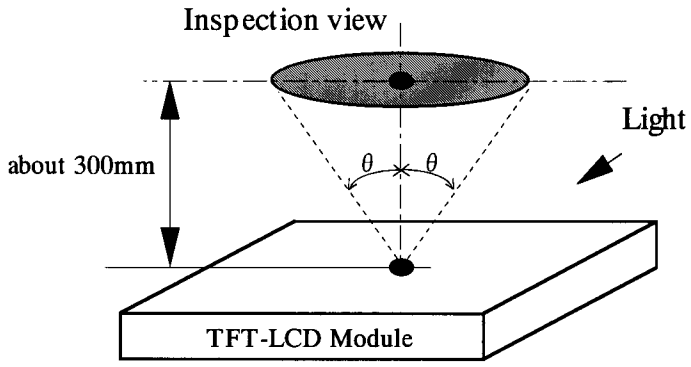
(1) Viewing zone

a) The figure shows the correspondence between eyes (of inspector) and TFT-LCD module.

$\theta \leqq 45^\circ$: when non-operating inspection

$\theta \leqq 5^\circ$: when operating inspection

b) Inspection should be executed only from front side and only A-zone.
Cosmetic of B-zone and C-zone are ignore.
(refer to 9.2 Definition of zone)



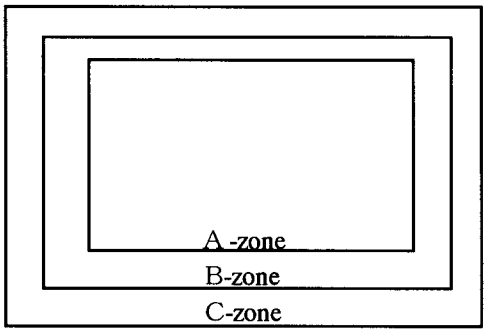
(2) Environmental

a) Temperature : 25 degrees

b) Ambient light : about 700 lx and non-directive when operating inspection.
: about 1000 lx and non-directive when non-operating inspection.

c) Back-light : when non-operating inspection, back-light should be off.

9.2 Definition of zone



- A-zone : Display area (pixel area)
- B-zone : Area between A-zone and C-zone
- C-zone : Metallic bezel area (include I/F connector)

9.3 COSMETIC SPECIFICATIONS

When displaying conditions are not stable (ex. at turn on or off), the following specifications are not applied.

	No.	ITEM			Max. acceptable number A-zone	Unit	Note
Operating inspection	1	Dot defect	Sparkle mode	1-dot	10	pcs	1),2),4)
				2-dots	3	Units	1),2),5)
				3-dots	1		
				4-dots	0		
				Density	3	pcs/ ϕ 20mm	1),2),6)
				Total	10	pcs	1),2)
			Black mode	1-dot	10	pcs	1),3),4)
				2-dots	3	Units	1),3),5)
				3-dots	1		
				4-dots	0		
				Density	3	pcs/ ϕ 20mm	1),3),6)
				Total	10	pcs	1),3)
				Total	15	pcs	1)
	2	Line defect			Serious one is not allowed.	—	—
	3	Uneven brightness					
	4	Stain inclusion [Line shape W : width (mm) L : length (mm)]	W≦0.02	L : Ignore	Ignore	pcs	7)
			W≦0.04	L≦2.0	10		
				L>2.0	0		
			W≦0.08	L≦1.0	10		
				L>1.0	0		
			W>0.08	—	(See dot shape)		
	5	Stain inclusion [Dot shape D : ave. dia. (mm)]	D≦0.22		Ignore	pcs	7)
			D≦0.4		5		
			D>0.4		0		
	6	Scratch on polarizer [Line shape W : width (mm) L : length (mm)]	W≦0.02	L : Ignore	Ignore	pcs	8)
			W≦0.08	L≦20	10		
				L>20	0		
			W>0.08	—	0		
	7	Scratch on polarizer [Dot shape D : ave. dia. (mm)]	D≦0.2		Ignore	pcs	8)
			D≦0.6		10		
			D>0.6		0		

	No.	ITEM		Max. acceptable number A-zone	Unit	Note
operating inspection	8	Bubbles, peeling in polarizer [D : ave. dia. (mm)]	D≦0.2	Ignore	pcs	8)
			D≦0.5	5		
			D>0.5	0		
non-operating inspection	9	Wrinkles on polarizer		Serious one is not allowed.	-	-

Note 1) Dot defect : defect area > 1/2 dot

2) Sparkle mode : brightness of dot is more than 30% at black. (visible to eye)

3) Black mode : brightness of dot is less than 70% at white. (visible to eye)

4) 1 dot : defect dot is isolated, not attached to other defect dot.

5) N dots : N defect dots are consecutive. (N means the number of defects dots)

6) Density : number of defect dots inside 20mm ϕ.

7) Those stains which can be wiped out easily are acceptable.

8) Polarizer area inside of B-zone is not applied.

9) No major (serious) defects when viewed in gray scale mode.

10. PRECAUTION

Please pay attention to the followings when a Super-TFT module with a back-light unit is used, handled and mounted.

10.1 Precaution to handling and mounting

(1) Applying strong force to a part of the module may cause partial deformation of frame or mold, and cause damage to the display.

(2) The module should gently and firmly be held by both hands. Never hold by just one hand in order to avoid any internal damage. Never drop or hit the module. Never push the surface of effective display area.

(3) The module should be installed with mounting holes at each corner of a module.

(4) Uneven force such as twisted stress should not be applied to a module when a module is mounted on the cover case. The cover case must have sufficient strength so that external force can not be transmitted directly to a module.

(5) It is recommended to leave a space between a module and a holding board of a module so that partial force is not applied to a module.

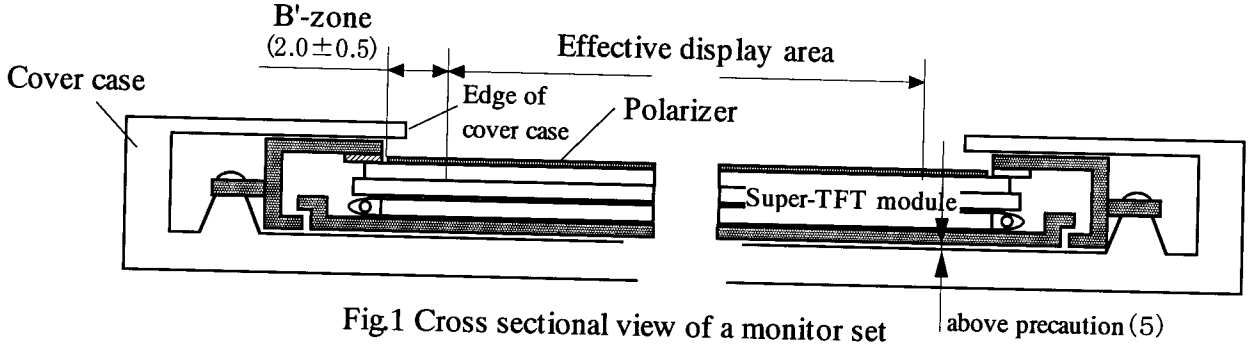


Fig.1 Cross sectional view of a monitor set

(6) The edge of a cover case should be located inside more than 1mm from the edge of a module front frame.

(7) A transparent protective plate should be added on the display area of a module in order to protect a polarizer and Super-TFT cell. The transparent protective plate should have sufficient strength so that the plate can not touch a module by external force.

(8) Materials included acetic acid and choline should not be used for a cover case as well as other parts and boards near a module. Acetic acid attacks a polarizer. Choline attacks electric circuits due to electro-chemical reaction.

(9) The polarizer on a TFT cell should carefully be handled due to its softness, and should not be touched, pushed or rubbed with glass, tweezers or anything harder than HB pencil lead. The surface of a polarizer should not be touched and rubbed with bare hand, greasy clothes or dusty clothes.

(10) The surface of a polarizer should be gently wiped with absorbent cotton, chamois or other soft materials slightly contained petroleum benzene when the surface becomes dirty. Normal-hexane as cleaning chemicals is recommended in order to clean adhesives which fix front/rear polarizers on a Super-TFT cell. Other cleaning chemicals such as acetone, toluen and alcohol should not be used to clean adhesives because they cause chemical damage to a polarizer.

(11) Saliva or water drops should be immediately wiped off. Otherwise, the portion of a polarizer may be deformed and its color may be faded.

(12) The module should not be opened or modified. It may cause not to operate properly.

(13) Metallic bezel of a module should not be handled with bare hand or dirty gloves. Otherwise, color of a metallic frame may become dirty during its storage. It is recommended to use clean soft gloves and clean finger stalls when a module is handled at incoming inspection process and production (assembly) process.

(14) Lamp(CCFL) cables should not be pulled and held.

10.2 Precaution to operation

(1) The ambient temperature near the operated module should be satisfied with the absolute maximum ratings. Unless it meets the specifications, sufficient cooling system should be adopted to system.

(2) The spike noise causes the mis-operation of a module. The level of spike noise should be as follows:
-200mV≦over- and under- shoot of VDD≦ +200mV
VDD including over- and under- shoot should be satisfied with the absolute maximum ratings.

(3) Optical response time, luminance and chromaticity depend on the temperature of a Super-TFT module. Response time and saturation time of CCFL luminance become longer at lower temperature operation.

(4) Sudden temperature change may cause dew on and/or in the a module. Dew males damage to a polarizer and/or electrical contacting portion. Dew causes fading of displayed quality.

(5) Fixed patterns displayed on a module for a long time may cause after-image. It will be recovered soon.

(6) A module has high frequency circuits. Sufficient suppression to electromagnetic interference should be done by system manufacturers. Grounding and shielding methods may be effective to minimize the interference.

(7) Noise may be heard when a back-light is operated. If necessary, sufficient suppression should be done by system manufacturers.

(8) The module should not be connected or removed while a main system works.

10.3 Electrostatic discharge control

(1) Since a module consists of a Super-TFT cell and electronic circuits with CMOS-ICs, which are very weak to electrostatic discharge, persons who are handling a module should be grounded through adequate methods such as a list band. I/F connector pins should not be touched directly with bare hands.

(2) Protection film for a polarizer on a module should be slowly peeled off so that the electrostatic charge can be minimized.

10.4 Precaution to strong light exposure

(1) A module should not be exposed under strong light. Otherwise, characteristics of a polarizer and color filter in a module may be degraded.

10.5 Precaution to storage

When modules for replacement are stored for a long time, following precautions should be taken care of:

(1) Modules should be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during storage. Modules should be stored at 5 to 35℃ at normal humidity (60%RH or less).

(2) The surface of polarizers should not come in contact with any other object. It is recommended that modules should be stored in the Hitachi's shipping box.

10.6 Precaution to handling protection film

(1) The protection film for polarizers should be pealed off slowly and carefully by persons who are electrically grounded with adequate methods such as a list band. Besides, ionized air should be blown over during peeling action. Dusts on a polarizer should be blown off by an ionized nitrogen gun and so on.

(2) The protection film should be peeling off without rubbing it to the polarizer. Because, if the film is rubbed together with the polarizer, since the film is attached to the polarizer with a small amount of adhesive, the adhesive may remain on a polarizer.

(3) The module with protection film should be stored on the conditions explained in 10.5 (1). However, in case that the storage time is too long, adhesive may remain on a polarizer even after a protection film is peeled off. Besides, in case that a module is stored at higher temperature and/or higher humidity, adhesive may remain on a polarizer. The remained adhesive may cause non-uniformity of display image.

(4) The adhesive can be removed easily with Normal-Hexane. The remained adhesive or its vestige on the polarizer should be wiped off with absorbent cotton or other soft materials such as chamois slightly contained Normal-Hexane.

10.7 Safety

(1) Since a Super-TFT cell and lamps are made of glass, handling to the broken module should be taken care sufficiently in order not to be injured. Hands touched liquid crystal from a broken cell should be washed sufficiently.

(2) A inverter located in rear side of a module can drive by high voltage. Super-TFT module has a plastic cover due to safety of high voltage.

(3) The module should not be taken apart during operation so that back-light drives by high voltage.

10.8 Environmental protection

(1) The Super-TFT module contains cold cathode fluorescent lamps. Please follow local ordinance or regulations for its disposal.

(2) Flexible circuits board and printed circuits board used in a module contain small amount of lead. Please follow local ordinance or regulations for its disposal.

10.9 Use restrictions and limitations

(1) This product is not authorized for use in life support devices or systems, military applications or other applications which pose a significant risk of personal injury.

(2) In no event shall Hitachi, Ltd., be liable for any incidental, indirect or consequential damages in connection with the installation or use of this product, even if informed of the possibility thereof in advance. These limitations apply to all causes of action in the aggregate, including without limitation breach of contact, breach of warranty, negligence, strict liability, misrepresentation and other torts.

10.10 Others

(1) Electrical components which may not affect electrical performance are subjective to change without notice because of their availability.